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Sir:

Under the provisions of 35 U.S.C. §119, filed herewith is a certified copy of European Patent Application No. 02 447 227.6, filed November 21, 2002, in accordance with the International Convention for the Protection of Industrial Property, 53 Stat. 1748, under which Applicant hereby claims priority.

Respectfully submitted,

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Exact self-calibration of a pll with multiphase clocks

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EXACT SELF-CALIBRATION OF A PLL WITH MULTIPHASE CLOCKS

Field of the invention

[0001] The present invention is related to a fractional-N frequency synthesizer used in digital communication systems. More precisely, it relates to a frequency synthesizer based on a Phase-Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used.

State of the art

[0002] In many applications, e.g. in mobile radio systems, it is necessary to synthesize frequencies in a digital way, i.e. using a Phase-Locked Loop. A conventional integer-N frequency synthesizer produces an output frequency that is N times the input reference frequency, such that its frequency resolution is the same as the PLL reference frequency. Therefore, narrow channel spacing is accompanied by a small loop bandwidth, which leads to long settling times. With a fractional-N frequency synthesizer an output frequency is generated that is N+X/Y times the input reference frequency, i.e. a fractional multiple of the reference frequency, such that narrow channel spacing is achieved along with a higher phase detector frequency. If Y is not too big the fractional-N frequency synthesizer can be based on multiphase clock signals. The Voltage Controlled Oscillator (VCO) then disposes of Y copies of the signal, each shifted over $2\pi/Y$. The value of X then

determines at which instances a VCO output pulse is generated.

[0003] Several major drawbacks arise from this approach. A mismatch between the various clock signal phases causes reduced quadrature accuracy, if the phases are used in an image-reject transceiver. Further, when the PLL is locked, the delay mismatches introduce periodic phase errors that give rise to fractional spurs in the output frequency spectrum, resulting in an out-of-spec transmitter spectrum and in a reduced interference capability in the receiver. A solution to this problem is suggested in IEEE JSSC, Vol. 36, No.5, May 2001, pp.777-783. It consists in adding to the PLL a self-calibrating loop to eliminate the delay mismatches. The calibration loop adjusts the phases of the multiphase clock signal based on the timing information present in the phase frequency detector (PFD) outputs. The calibration loop has a much smaller bandwidth in order to avoid disturbance of the locking behaviour of the main loop. A safe solution here is to activate the calibration loop only when the main loop is locked. In the calibration loop there is a multiplexing switch that guides the current coming out of the calibration charge pump towards one of the Y calibration loop filters. Which one of the Y calibration loop filters is to be selected, is determined by a control logic that knows which phase is currently selected by the phase-switching fractional divider and thus knows which phase must be calibrated.

[0004] Still the problem remains that a mismatch between the main charge pump of the original loop and the calibration charge pump of the calibration loop will result in an incorrect compensation of the phase errors. Therefore, the quadrature accuracy is still not correct yet and the fractional spurs are not completely removed.

Aims of the invention

[0005] The present invention aims to propose a product that synthesizes a fractional-N frequency based on a Phase-Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used in such a way that mismatch problems between the two charge pumps are avoided.

Summary of the invention

[0006] The present invention is related to a Phase-Locked Loop with multiphase clocks with

- a main loop comprising a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider, coupled in cascade,
- a calibration loop comprising Y Calibration Loop Filters, with Y being an integer, coupled with its output to said Multi-Phase Voltage Controlled Oscillator (VCO), and a Control Logic arranged to control said Phase-Switching Fractional Divider,
- a Reference Frequency Signal applied to said Phase Frequency Detector.

[0007] The Phase-Locked Loop comprises a Multiplexer between the output of said Main charge pump and the inputs of both said main loop filter and said Y calibration loop filters, and is arranged to receive a control signal from said control logic, and wherein a Calibration signal applied at a control input of said Control Logic.

[0008] As a second object the present invention is related to a method for synthesizing frequencies with a Phase-Locked Loop with multiphase clocks.

[0009] According to a first preferred embodiment of the invention, the PLL is part of a fractional-N frequency

synthesizer.

[0010] According to a second preferred embodiment of the invention the Phase-Locked Loop can be comprised in an integrated circuit.

[0011] Advantageously, the Phase-Locked Loop can be part of a digital mobile radio communication system.

Short description of the drawings

[0012] Fig. 1 represents the prior art solution.

[0013] Fig. 2 represents the invention.

Detailed description of the invention

[0014] The present invention relates to a Phase-Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used. In order to avoid any mismatch problems between the main charge pump of the original loop and the calibration charge pump of the calibration loop, the same main charge pump is used for both loops.

[0015] The prior art solution is depicted in Fig.1. A first (Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD)(1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (VCO)(4) and a Phase-switching Fractional Divider (5). A second loop (Calibration) comprises the series connection of a Calibration Charge Pump (9), a Multiplexer (6) and Y Calibration Loop Filters (7), with Y being an integer, coupled between said Phase Frequency Detector (PFD)(1) and said Multi-Phase Voltage Controlled Oscillator (VCO)(4). The Multiplexer (6) is controlled by a Control Logic (8) coupled to the Phase-Switching Fractional Divider (5). A Reference Frequency Signal (10) is being applied to said Phase Frequency Detector (1). The Calibration signal (11) is applied to a control input of the Control Logic (8).

[0016] The main charge pump is denoted by (2) in Fig.2. The control logic (8) must master the multiplexer (6) in such a way that most of the time the main loop filter is chosen and sometimes one of the calibration loop filters is chosen. Most of the cycles of this charge pump are indeed used for the main loop, which has the highest bandwidth. In this state multiplexer (6) is just a through connection. However, from time to time, a cycle of the charge pump current is taken from the main loop and used for the calibration loop. When this occurs, the multiplexer (6) guides the current towards one of the filters (7). Which filter exactly is chosen, is determined by the state the phase-switching fractional divider is in.

[0017] Fig. 2 shows the two loops in the system. A first (Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD)(1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (VCO)(4) and a Phase-switching Fractional Divider (5). A second loop (Calibration) comprises the series connection of a Multiplexer and Y Calibration Loop Filters, with Y being an integer, coupled between said Phase Frequency Detector (PFD) (1) and said Multi-Phase Voltage Controlled Oscillator (VCO) (4). The multiplexer (6) is controlled by a Control Logic (8) coupled to the Phase-Switching Fractional Divider (5), and a Reference Frequency Signal (10) is being applied to said Phase Frequency Detector (1).

[0018] The multiplexer (6) has an input connected to an output of the Main Charge Pump (2), and has outputs connected to inputs of the Main Loop Filter (3) and of Y Calibration Loop Filters (7). The Calibration signal (11) is applied to a control input of the Control Logic (8).

[0019] A practical example might be that, for Y=8, one out of nine cycles is used for calibration.

- Suppose we want to divide by N+1/8. In this case the phase switching divider output is subsequently aligned with phase 1-2-3-4-5-6-7-8-1-2-3-4-... Therefore the multiplexer sequence shown in the left hand part of the table below can be used, where M denotes the main loop and Cx calibration loop x, with x = 1 to 8.
- Suppose we want to obtain a division by N+2/8. Then the phase switching divider output is subsequently aligned with phase 1-3-5-7-1-3-5-7-1-3-... This leads the multiplexer sequence in the right hand part of the table.

N+1/8			N+2/8		
index	**phase**	**loop**	**index**	**phase**	**loop**
1	1	M	1	1	M
2	2	M	2	3	M
3	3	M	3	5	M
4	4	M	4	7	M
5	5	M	5	1	M
6	6	M	6	3	M
7	7	M	7	5	M
8	8	M	8	7	M
9	1	C1	9	1	C1
10	2	M	10	3	M
11	3	M	11	5	M
12	4	M	12	7	M
13	5	M	13	1	M
14	6	M	14	3	M
15	7	M	15	5	M
16	8	M	16	7	M
17	1	M	17	1	M
18	2	C2	18	3	C3
19	3	M	19	5	M
...					

[0020] The PLL described above can advantageously be applied in a fractional-N frequency synthesizer. In this way the spurious problems are completely removed and, moreover, the result does no longer rely on accurate

matching of components. Further, the I/Q accuracy is greatly improved.

CLAIMS

1. A Phase-Locked Loop with multiphase clocks comprising:

- a main loop comprising a Phase Frequency Detector (1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (4) and a Phase-switching Fractional Divider (5) coupled in series,
- a calibration loop comprising Y Calibration Loop Filters (7), with Y being an integer, coupled with its output to said Multi-Phase Voltage Controlled Oscillator (4), and a Control Logic (8) arranged to control said Phase-Switching Fractional Divider (5), and
- a Reference Frequency Signal (10) applied to said Phase Frequency Detector (PFD)(1)

characterised in that the Phase-locked loop comprises a Multiplexer (6) between the output of said Main charge pump (2) and the inputs of both said main loop filter (3) and said Y calibration loop filters, and is arranged to receive a control signal from said control logic, and wherein a Calibration signal (11) applied at a control input of said Control Logic (8).

2. A method for synthesizing frequencies with a Phase-Locked Loop with multiphase clocks, comprising the following steps :

- Providing a Phase-Locked Loop such as in claim 1
- Applying a reference frequency signal (10) to the Phase Frequency Detector (1) of the Phase-Locked Loop, and
- Applying a Calibration Signal (11) to the Control Logic (8) of the Phase-Locked Loop.

3. A fractional-N frequency synthesizer comprising a Phase-Locked Loop as in claim 1 or implementing the method of claim 2.

4. An integrated circuit comprising a Phase-Locked Loop as in claim 1.

5. A digital mobile radio communication apparatus comprising a Phase-Locked Loop as in claim 1 or implementing the method of claim 2.

ABSTRACT

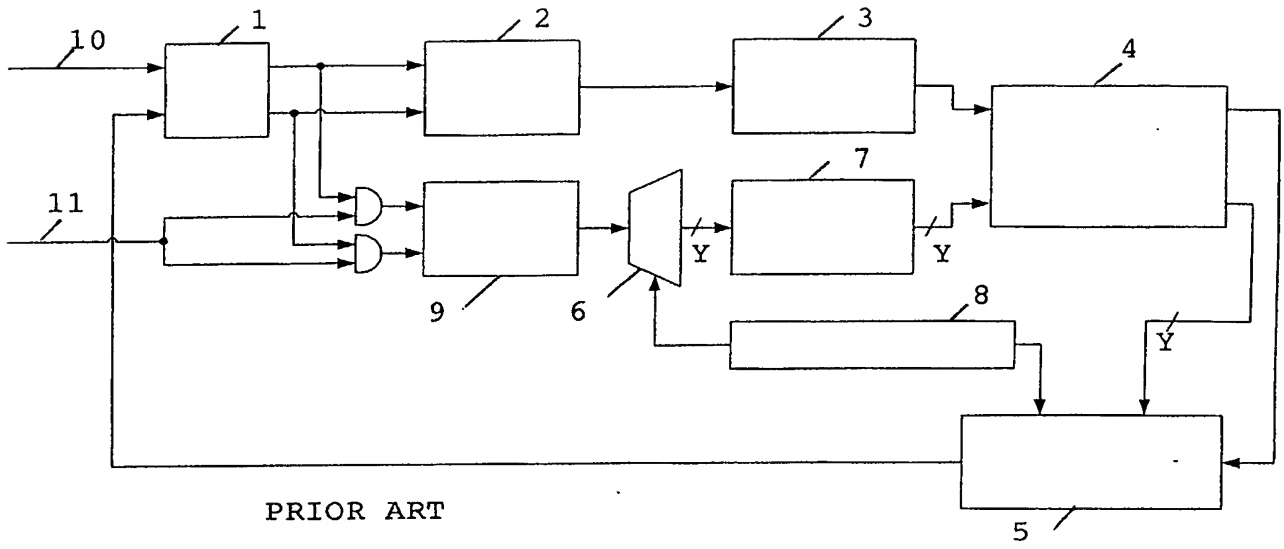
EXACT SELF-CALIBRATION OF A PLL WITH MULTIPHASE CLOCKS

The present invention is related to a Phase-Locked Loop with multiphase clocks with

- a first loop (Main loop) comprising, coupled in cascade, a Phase Frequency Detector (PFD)(1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (VCO) (4) and a Phase-switching Fractional Divider (5), and
- a second loop (for Calibration) comprising the series connection of a Multiplexer (6) and Y Calibration Loop Filters (7), with Y being an integer, coupled between said Phase Frequency Detector (PFD) (1) and said Multi-Phase Voltage Controlled Oscillator (VCO)(4), said Multiplexer (6) being controlled by a Control Logic (8) coupled to said Phase-Switching Fractional Divider (5), and a Reference Frequency Signal (9) being applied to said Phase Frequency Detector (PFD)(1),

characterised in that said Multiplexer (6) has an input connected to an output of said Main Charge Pump (2), and has outputs connected to inputs of said Main Loop Filter (3) and of said Y Calibration Loop Filters (7),
and in that a Calibration signal (10) is applied at a control input of said Control Logic (8).

(Figure 2)



PRIOR ART

FIG. 1

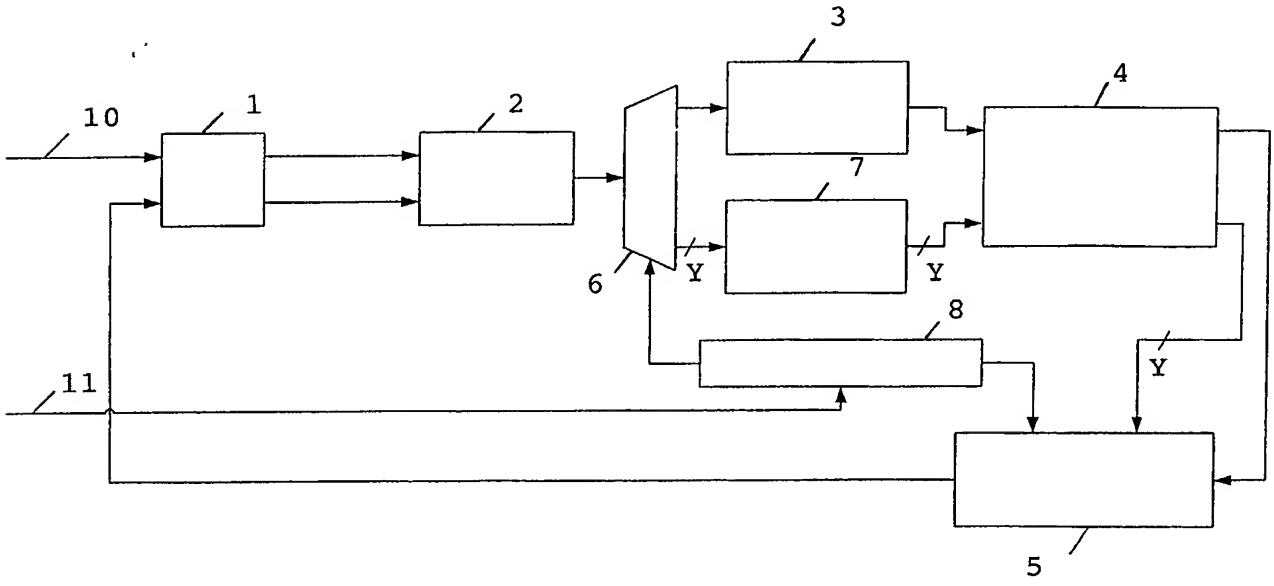


FIG. 2